REMARKS

Claims 1-12 remain pending in the application. The specification and claims 1, 2, 4, 8, and 10 have been amended without introduction of new matter. Favorable reconsideration is respectfully requested in view of the above amendments and the following remarks.

A number of the drawings were objected to as failing to comply with 37 C.F.R. §1.84(p)(5) because they allegedly include reference signs not mentioned in the description.

With respect to the letter "H" found in Figure 13, the Office's attention is directed to the specification at page 18, lines 23-26 which reads "In step H, a transaction grant message is ... ." As the reference character in question (i.e., "H") is in fact referred to in the specification, no change is believed to be required.

As to the remaining reference characters identified in the Action, Applicants have now corrected the informality by amending the specification to mention the reference characters. No new matter has been introduced.

The drawings were further objected to as failing to comply with 37 C.F.R. §1.84(p)(4) because reference character "A" has been used to designate both "start" in Figure 13 and "assign initial stack positions" on page 17, lines 25-27; because reference character "B" has been used to designate both "assign initial stack positions" in Figure 13 and "receive respective transaction requests" on page 17, line 32 through page 18, line 2; and because reference character "C" has been used to designate both "receive transaction request" in Figure 13 and "determine highest priority level" on page 18, lines 5-8.

In response, Applicants note that when comparison is made with the corresponding description from page 17, line 25 to page 18, line 11, it is evident that the discrepancies that form the bases for these objections have arisen in the description rather than in the drawings. In particular, step A has been incorrectly identified as "assign initial stack positions" rather than "Start" and this has upset the referencing to subsequent stages B and C, whereas reference to step D has been inadvertently omitted altogether. Thus, instead of amending Figure 13 (which is believed to be correct), Applicants consider it more appropriate to correct the description as follows:

On page 17, line 25, immediately before the first sentence, beginning "The initial set up of the arbitration scheme ...", the following sentence has been added: "The arbitration scheme starts at step A."

On page 17, lines 25-27, the sentence has been amended to read: "The initial set up of the arbitration scheme is to arrange the modules into initial stack positions (step [[A]] B) which are stored in the stack storage means 26."

On page 17, line 32 through page 18, line 2, the sentence has been amended to read as follows: "In step [[B]] C, the arbitration unit 21 receives respective transaction requests from any number of the modules M1 to M5."

And, on page 18, line 11, before the sentence beginning "The control means then masks ..." the following sentence has been inserted: "In step D, the control means obtains the highest priority transaction request."

With these amendments, all reference characters appearing in the figures are also believed to be mentioned in the specification, and the reference characters used in Figure 13 are believed to be compatible with their use in the description. Accordingly, it is respectfully requested that the objections to the figures under 37 C.F.R. §§ 1.84(p)(4)-(5) be withdrawn.

Claims 4, 7, 8, and 10 were objected to because of a number of informalities. To address these informalities, the word "or" that appears in claim 4 at line 32 has been changed to "of"; and the word "any" that appears in claim 10 at line 25 has been cancelled. These changes are believed to address all of the Office's concerns with respect to the objection. Consequently, it is respectfully requested that the objection to the claims be withdrawn.

Claims 1-12 were rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. This rejection is respectfully traversed.

Claim 1 is rejected on the basis that it is not clear if the "bus connection units" of line 10 refer to the same units as the "bus connecting unit" of lines 13-14. The specification (see for instance page 7) has otherwise consistently referred to these units as "bus connection units". This clerical error has therefore been corrected by replacing the word "connecting" in line 14 of claim 1 with the word "connection".

Claim 2 is objected to on the basis that it is unclear as to what attributes the output circuitry is optimized for. Support for this feature can be found in the description of a preferred implementation of the invention on page 30, lines 17-28, where it is made clear that the output circuitry is tailored for the particular length of bus between it and the next connection module so that the signal characteristics along the bus are optimized. Claim 2 has accordingly been amended to recite "tailored to optimize the signal characteristics for the length of the bus portions concerned." The skilled person would understand the factors involved in matching a line portion to a connected unit and would therefore appreciate the

parameters that need to be considered to ensure that the characteristics for a particular section of line (portion) are optimized for the properties of the signal(s) being transmitted.

Claim 8 is rejected on the grounds that it is unclear where the term "one pipeline stage" as used in line 19 of claim 8 is defined. It is believed that this objection has now been overcome by removing the reference to an earlier definition and replacing it with wording defining the meaning within the claim itself. In particular, claim 8 has been amended to now define "Apparatus as claimed in claim 4, wherein the primary bus [[is]] has a length of one pipeline stage, ~~as herein defined, in length~~ said length being the bus length traveled by a data pulse in a single system clock cycle."

Support for this amendment may be found, for example, in the list of definitions appearing in the specification at page 10, lines 12 to 13.

Claim 10 is rejected on the grounds that the nature of the "separate" read, write and transaction buses is unclear. This concern has been addressed by amending claim 10 to make it clear that the bus architecture comprises separate read, write and transaction buses (consistent with the description in pages 13-15 and as illustrated in Figure 5, for example), thereby removing any suggestion that the claim could be interpreted in the sense that the read, write and transaction buses are separate from the pipeline bus architecture.

In view of the above, claims 1-12 are believed to define the claimed subject matter with sufficient particularity and distinctness to satisfy the terms of the statute. Accordingly, it is respectfully requested that the rejection of claims 1-12 under 35 U.S.C. §112, second paragraph, be withdrawn.

Claims 1, 2, 3, 5, and 12 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over "Automatic High Level Synthesis of Partitioned Busses" by Christian Ewering ("Ewering") and U.S. Patent Number 5,920,894 to Plog et al. ("Plog"). This rejection is respectfully traversed.

In the present application, problems of latency in particular are addressed in the context of a computer system in a number of ways. Part of the solution is the design of bus architecture that the computer system employs. It becomes necessary to consider different facets of the overall solution, depending on that architecture. In independent claim 1 as presented, the combination of bus connection units, each including multiplexer circuitry for selectively connecting a module to a section of a pipelined bus architecture, in which data traverses that architecture over a plurality of system clock cycles, is not actually disclosed in

Ewering. Moreover, there is nothing in Ewering alone or in combination with Plog that would suggest the claimed combination to the person of ordinary skill in the art.

Considering Ewering in more detail, Figure 1 shows a segmented bus architecture in which serial segments 1.0. 1.1 etc and 0.0, 0.1 etc (corresponding to partitions 0 and 1) are interconnected by switches. These switches "permit[] or inhibit[] the flow of data from one segment to another" as stated in page 304 in the paragraph headed "2. Target Architecture". In other words, these switches appear to be capable of isolating one segment from another. It also appears that there are "modules" connected to the bus architecture, each module consisting of registers and an ALU with input and output buffers. However, these "modules" are connected directly to the respective segmented buses and not via the switches. The switches play no part in the connection of the modules to the bus segments. Indeed, they play the completely different role of enabling or permitting data transfer along the bus structure. It is accepted that the "modules" would be connected to the bus segments somehow but there is no disclosure or suggestion in Ewering that such connections would comply with the requirements of claim 1. Ewering is in fact completely silent as to the manner and means of connecting the modules to the bus segments.

When this is compared to Applicants' claim 1, it becomes immediately clear that there are significant and patentable differences. Thus, claim 1 requires a pipeline bus structure comprising a plurality of bus portions connected in series by bus connection units. In order to map these features to Ewering, it would require the switches in Ewering to be regarded as the bus connection units since they are the only means for connecting the Ewering bus segments to one another. In Applicants' description it is made clear that the bus connection units provide a facility in which the characteristics of the bus segments are preserved independently of the presence or absence of a module connected to a bus connection unit – see page 30, lines 17-28. This clearly cannot be the case in Ewering since, to all intents and purposes, if a Ewering switch is operated to prevent data transfer, the relevant bus segment is isolated from the remainder of the bus structure.

Applicants' claim 1 goes further in requiring each module to be connected to the bus architecture by way of a respective one of the bus connection units. That is simply not the case in Ewering where, as just discussed, the Ewering modules are connected directly to the bus segments and not via the switches. Moreover, the switches in Ewering are specifically provided to permit or deny data transfer, as previously mentioned, so they are more akin to an on/off switch than to a multiplexer. On that basis alone, there would be no reason for a

person skilled in the art even to contemplate using a multiplexer in place of a switch that is not in any case performing the same function.

Further, claim 1 specifically requires that data traverses the pipelined bus architecture over a plurality of system clock cycles. There is no mention of this in Ewering, so Ewering is even more remote from claim 1 in respect of this feature, in addition to the other features discussed in the preceding paragraphs. The advantage of such feature is that the data flow is regulated at each stage of the bus, thereby improving overall control of data handling throughout the bus and throughout the system of which the bus may form a crucial part. Setting aside for the moment the multiplexer feature, the feature of the data traversing the pipelined bus architecture over a plurality of system clock cycles, in combination with (i) the pipelined bus structure itself and (ii) the bus connection units, is itself a significant and patentable distinction over Ewering.

Plog fails to make up for the deficiencies of Ewering. Plog provides a circuit arrangement enabling two processors, one of which is of higher rank than the other, to access a common memory. In this way, one processor can be processing already accessed data while the other is accessing the memory (see the abstract). The Plog invention is aimed at reducing waiting time, especially in write operations, when the higher rank processor interrupts the lower rank processor. In Figure 1 of Plog, a control circuit 12 controls access to the memory 10 via a multiplexer 22 which is connected to the address registers 14, 18 of the processors, not shown in the drawings. The multiplexer is therefore used solely to arbitrate, or control, accesses to the common memory. Thus far, Plog gives no hint or suggestion that the multiplexer could be used for connecting the processors to any of the buses 24-26 and 28-30. Indeed, in column 4, lines 20-26, Plog states that the multiplexer could be replaced by tri-state buses connected directly to the address bus 23 of the memory 10. The multiplexer is therefore of insignificant interest in the Plog circuit arrangement. It should also be carefully noted that the buses shown in Figure 1 are those connecting the circuit arrangement to the processors and to the memory. Those buses are not segmented and there is no hint that they could be segmented or partitioned as required in applicant's claim.

Figure 2 of Plog describes a practical implementation of a data register designed to accommodate the fact that the memory data word width is half that of the processor data word width (i.e., 8-bit for the memory compared to 16-bit for the processors - see column 5, line 10 to column 6, line 11). In essence, the write data register is split into two parts 50, 52, each of a width capable of handling the memory data words. Write data words are routed

through the two parts 50, 52 via a multiplexer 54 under the control of a lead 29a of the control bus 29. The passage specifically indicated by the Office, namely column 5, lines 50-54, states that "the two registers 50, 52 can instead be connected in parallel to the input 30, in which case the multiplexer 54 selectively connects one of the outputs of the registers 50 or 52 to the data bus 11".

Bearing in mind that this data bus 11 is a bus internal to the circuit arrangement of Figure 1 and is not part of a segmented bus architecture providing communication between a plurality of modules connected to the bus architecture, it is inconceivable that the person of ordinary skill would contemplate adapting the teaching in Plog to the system in Ewering, which itself does not contain the remaining components of the system defined in Applicants' claim. Plog has absolutely nothing to do with data buses. Any disclosure in Plog of multiplexers is simply to control access to one or other of two "half-registers" within a circuit arrangement quite separate from the main data bus of, for example, a data processor.

In view of the foregoing, it is therefore respectfully submitted that Ewering and Plog together do not render Applicants' claim 1 obvious, nor would do these references considered individually or in combination render obvious any of claims 2, 3, 5, and 12, which variously depend from claim 1. It is therefore respectfully requested that the rejection of claims 1, 2, 3, 5, and 12 under Section 103 be withdrawn.

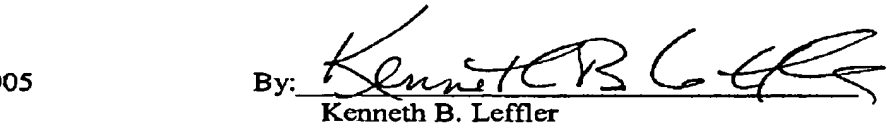
Claims 4, 6, 7, and 8 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Ewering and Plog as applied to claims 1 and 5 above, and further in view of U.S. Patent Number 5,627,976 to McFarland et al. ("McFarland"). Claim 9 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Ewering and Plog as applied to claim 1 above, and further in view of U.S. Patent Number 5,128,926 to Perlman et al. ("Perlman"). Claims 10 and 11 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Ewering and Plog as applied to claim 1 above, and further in view of U.S. Patent Number 5,925,118 to Revilla et al. ("Revilla").

In view of the arguments set forth above in support of Applicant's earnest contention that the claims 1 and 5 are novel and non-obvious, it is respectfully submitted that the further rejections relating to the alleged obviousness of claims 4, 6, 7 and 8 in the face of McFarland, the alleged obviousness of claim 9 in the face of Perlman, and the alleged obviousness of claims 10 and 11 in the face of Revilla are now all moot and require no specific attention in this response. It is accordingly respectfully requested that the rejection of claims 4, 6-8, 9, and 10-11 under Section 103 be withdrawn.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,
Potomac Patent Group PLLC

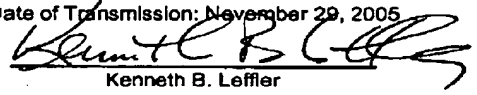
Date: November 29, 2005

By: 
Kenneth B. Leffler
Registration No. 36,075

P.O. Box 270
Fredericksburg, Virginia 22404
703-718-8884

I hereby certify that this correspondence is being sent by facsimile transmission to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 to the following facsimile number:

Facsimile Number: 571 273 8300
Date of Transmission: November 29, 2005


Kenneth B. Leffler